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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/981.957	10/16/2001	Brian James Misek	10010215-1	7262

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EXAMINER	
LUU, THANH X	

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 08/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/981,957	MISEK, BRIAN JAMES	
	Examiner	Art Unit	
	Thanh X. Luu	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,5-8,11,14-17 and 22-31* is/are pending in the application.

4a) Of the above claim(s) *31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,5-8,11,14-17 and 22-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the Appeal Brief filed on July 20, 2006, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

Claims 3, 5-8, 11, 14-17 and 22-31 are currently pending. Claim 31 has been withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 3, 5, 8, 11, 14, 17 and 22-30 are rejected under 35 U.S.C. 102(e) as

being anticipated by Panicacci et al. (U.S. Patent 6,885,396).

Regarding claims 3, 5, 8, 22, 25, 27 and 28, Panicacci et al. disclose (see Figs. 2 and 4A) a system comprising: an array of photocells (see Fig. 2) that are arranged in rows and columns; and a sequential readout circuit for sequentially reading out the value of the photocells on photocell at a time, comprising: a first sampling circuit (C1 of circuit 60A) that includes a first electrode (upper plate of capacitor) for coupled to a first column (from 49A) and a second electrode (lower plate of capacitor connected to ground); a first switch (S1 of circuit 60A) that includes a first electrode (see col. 5, lines 45-50; a transistor switch inherently has first, second and third electrodes as claimed) coupled to the second electrode of the first sampling circuit, a second electrode and a third electrode for receiving a first sample control signal (signal for operating transistor switch; not shown), wherein the first switch selectively couples the first electrode of the first switch to the second electrode of the first switch when the first sample control signal is asserted (inherently, this is what happens when a transistor switch is closed), wherein (see col. 6, lines 25-50) the first sampling circuit samples a light signal (pixel value) and a reset signal (reset value) from each photocell in the first column; a second sampling circuit (C1 of circuit 60B) that includes a first electrode for coupling to a second column and a second electrode; a second switch (S1 of circuit 60B) that includes a first electrode coupled to the second electrode of the second sampling circuit, a second electrode, and a third electrode for receiving a second sample control signal, wherein the second switch selectively couples the first electrode of the second switch to the second electrode of the second switch when the second sample control signal is

asserted, wherein the second sampling circuit samples a light signal and a reset signal from each photocell in the second column; an amplifier (90) that includes a negative input terminal coupled to the second electrode of the first switch and the second electrode of the second switch, wherein the amplifier includes an output terminal for generating a signal that corresponds to the amount of light received by a particular photocell in the array. Panicacci et al. further disclose (see col. 7, lines 60-65) determining a difference between the light signal (Vsignal) and the reset signal (Vreset) for each photocell in the array in a time sequential manner; an integrating capacitor (C6) as claimed; and a photocell circuit (50A) as claimed.

Regarding claims 11, 14, 17, 23, 24, 26, 29 and 30, Panicacci et al. disclose (see Fig. 4A) a sequential readout circuit for coupling to an array of photocells that includes a plurality of photocells that are arranged in rows and columns, each photocell generating a light signal during a first period of time that represents received light and a reset signal after being reset, the circuit comprising: a first sampling circuit (C1 of circuit 60A) that includes a first electrode (upper plate of capacitor) for coupled to a first column (from 49A) and a second electrode (lower plate of capacitor connected to ground); a first switch (S1 of circuit 60A) that includes a first electrode (see col. 5, lines 45-50; a transistor switch inherently has first, second and third electrodes as claimed) coupled to the second electrode of the first sampling circuit, a second electrode and a third electrode for receiving a first sample control signal (signal for operating transistor switch; not shown), wherein the first switch selectively couples the first electrode of the first switch to the second electrode of the first switch when the first sample control signal

is asserted (inherently, this is what happens when a transistor switch is closed), wherein (see col. 6, lines 25-50) the first sampling circuit samples a light signal (pixel value) and a reset signal (reset value) from each photocell in the first column; a second sampling circuit (C1 of circuit 60B) that includes a first electrode for coupling to a second column and a second electrode; a second switch (S1 of circuit 60B) that includes a first electrode coupled to the second electrode of the second sampling circuit, a second electrode, and a third electrode for receiving a second sample control signal, wherein the second switch selectively couples the first electrode of the second switch to the second electrode of the second switch when the second sample control signal is asserted, wherein the second sampling circuit samples a light signal and a reset signal from each photocell in the second column; an amplifier (90) that includes a negative input terminal coupled to the second electrode of the first switch and the second electrode of the second switch, wherein the amplifier includes an output terminal for generating a signal that corresponds to the amount of light received by a particular photocell in the array. Panicacci et al. further disclose (see col. 7, lines 60-65) determining a difference between the light signal (Vsignal) and the reset signal (Vreset) for each photocell in the array in a time sequential manner; an integrating capacitor (C6) as claimed; and a photocell circuit (50A) as claimed.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6, 7, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Panicacci et al. in view of Simerly et al. (U.S. Patent 5,982,424).

Regarding claims 6, 7, 15 and 16, Panicacci et al. disclose the claimed invention as set forth above. Panicacci et al. do not specifically disclose a level shifting or gain manipulation circuit as claimed. Simerly et al. teach (see col. 7, lines 35-47) level shifting and gain manipulating in a similar system. Simerly et al. further recognize that level shifting and gain manipulation accounts for variations in dynamic ranges among frames. Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide such a configuration in the apparatus of Panicacci et al. in view of Simerly et al. to improve detection as taught.

Response to Arguments

6. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh X. Luu whose telephone number is 571-272-2441. The examiner can normally be reached on M-F 6:00AM-3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on 571-272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thanh X Luu
Primary Examiner
Art Unit 2878

08/2006